REMARKS

Claims 1, 3-6 and 8-19 are pending in the present application. Claims 1, 3-6 and 8 have been amended. Claims 10-19 have been presented herewith. Claims 2 and 7 have been canceled.

Priority Under 35 U.S.C. 119

A certified copy of Japanese Priority Application No. 2003-371729 has been submitted concurrently herewith. **The Examiner is respectfully requested to acknowledge receipt of the certified copy of Japanese Priority Application No. 2003-371729, and to confirm that the Claim for Priority under 35 U.S.C. 119 is complete**.

Drawings

Enclosed is one (1) red-inked Annotated Sheet, wherein Figs. 4(A) and 4(B) have been corrected so that the silicon substrate and the field oxide film have been clearly denoted respectively as 110 and 120. Also enclosed is one (1) drawing Replacement Sheet incorporating the above noted corrections. **The Examiner is respectfully requested to acknowledge receipt and acceptance of the above noted drawing Replacement Sheet.**

Claim Rejections-35 U.S.C. 103

Claims 1-5 and 9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Shinohara reference (U.S. Patent No. 6,245,603) in view of the Arima et al. reference (U.S. Patent No. 5,489,791) and the Oda et al. reference (U.S. Patent No. 5,945,710). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 1 includes in combination a source and a drain "both of a second conductivity type, formed on the surface of the semiconductor substrate, the source and the drain having a first depth from the surface of the semiconductor substrate"; a source side impurity layer "of the first conductivity type formed so as to extend from inside the source at a second depth that is shallower than the first depth, to directly underneath the gate electrode at a third depth that is equal to or deeper than the first depth"; and a drain side impurity layer "of the first conductivity type formed so as to extend from inside the drain at the second depth to directly underneath the gate electrode at the third depth". Applicant respectfully submits that the semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has presumably interpreted P-type ion implantation region 120 as shown in Figs. 3A and 4A – 4C of the Shinohara reference as a source side impurity layer and/or a drain side impurity layer of claim 1. However, as particularly clear in view of Fig. 4A of the Shinohara reference, P-type ion implantation region 120 does not extend from inside a source or drain region at a second depth that is shallower than a

first depth of the source or drain region, to directly underneath the gate electrode at a third depth that is equal to or deeper than the first depth of the source or drain region. As may be readily understood in view of Fig. 4A of the Shinohara reference, P-type ion implantation region 120 extends horizontally along a same depth from inside N-type ion implantation region 123 to a channel region outside N-type ion implantation region 123.

The Examiner has secondarily relied upon the Arima et al. and Oda et al. references. However, Figs. 2A – 2H of the Arima et al. reference as specifically relied upon by the Examiner do not include a source side impurity layer or a drain side impurity layer of a first conductivity type extending from within a source or a drain of a second conductivity type, to a channel region outside the source or drain. Particularly, Fig. 2D of the Arima et al. reference includes n^- impurity regions 43 and n^+ impurity regions 44 which constitute source/drain regions. Fig. 2H also illustrates n^- impurity regions 43 and 33c. Clearly, the Arima et al. reference as relied upon by the Examiner does not include source and drain side impurity layers as featured in claim 1.

Likewise, Figs. 15 and 16 of the Oda et al. reference include first and second lightly doped n-type source and drain regions 6c and 6d, and n-type high impurity contact region 11. Figs. 15 and 16 of the Oda et al. reference do not include a source side impurity layer or a drain side impurity layer of a first conductivity type extending from within a source or a drain of a second conductivity type, as would be necessary to meet the features of claim 1. Figs. 17 and 23 of the Oda et al. reference similarly fail to disclose or illustrate source and drain side impurity layers that would meet the features

of claim 1.

Applicant therefore respectfully submits that the Arima et al. and Oda et al. references as secondarily relied upon by the Examiner do not overcome the above noted deficiencies of the Shinohara reference. Applicant therefore respectfully submits that the semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 1 and 3 is improper for at least these reasons.

The process of fabricating a semiconductor device of claim 4 includes in combination "forming a source side impurity layer and a drain side impurity layer by introducing a dopant of the first conductivity type into the semiconductor substrate through the surface covering film and into the exposed surface of the semiconductor substrate near the gate electrode". As further featured, "the source side impurity layer extends from inside the source at a second depth that is shallower than the first depth, to directly underneath the gate electrode at a third depth that is equal to or deeper than the first depth, and wherein the drain side impurity layer extends from the drain at the second depth to directly underneath the gate electrode at the third depth".

Applicant respectfully submits that the process of fabricating a semiconductor device of claim 4 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least somewhat similar reasons as set forth above with respect to claim 1. P-type ion implantation region 120 of the Shinohara reference does not extend from within source or drain regions to regions underneath a

gate electrode at the depths as featured in claim 4. Moreover, the Arima et al. and Oda et al. references as secondarily relied upon by the Examiner do not disclose source and drain side impurity layers as would be necessary to meet the features of claim 4. Applicant therefore respectfully submits that the process of fabricating a semiconductor device of claim 4 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 4, 5 and 9 is improper for at least these reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. However, Applicant respectfully submits that claims 6 and 8 distinguish over the prior art at least by virtue of dependency upon claim 4 for the reasons as set forth above, and that amendment of claims 6 and 8 to be in independent form is therefore unnecessary.

Claims 10-19

Applicant respectfully submits that claim 10, as dependent upon claim 4, distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least the same reasons as set forth above with respect to claim 4, and by further reason of the features therein.

The semiconductor device of claim 11 includes in combination a source and a drain "formed on the surface of the semiconductor substrate, the source and the drain having a second conductivity type and a first depth from the surface of the semiconductor substrate"; and a pair of pocket regions "having the first conductivity type, formed in the semiconductor substrate, the pocket regions respectively extending from inside the source and the drain at a second depth that is shallower than the first depth, to underneath the gate electrode at a third depth that is equal to or deeper than the first depth". Applicant respectfully submits that the semiconductor device of claim 11 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least somewhat similar reasons as set forth above.

Conclusion

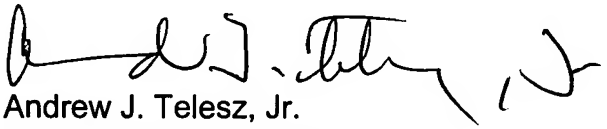
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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Enclosures: One (1) red-inked Annotated Sheet
One (1) drawing Replacement Sheet

ANNOTATED SHEET

F-03ED0083

FIG. 4(A)

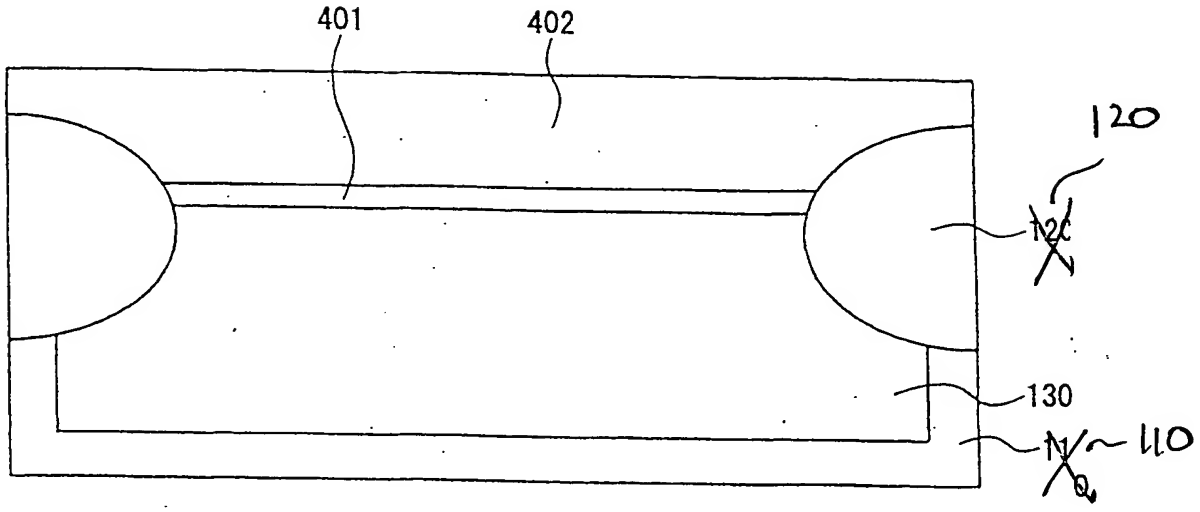


FIG. 4(B)

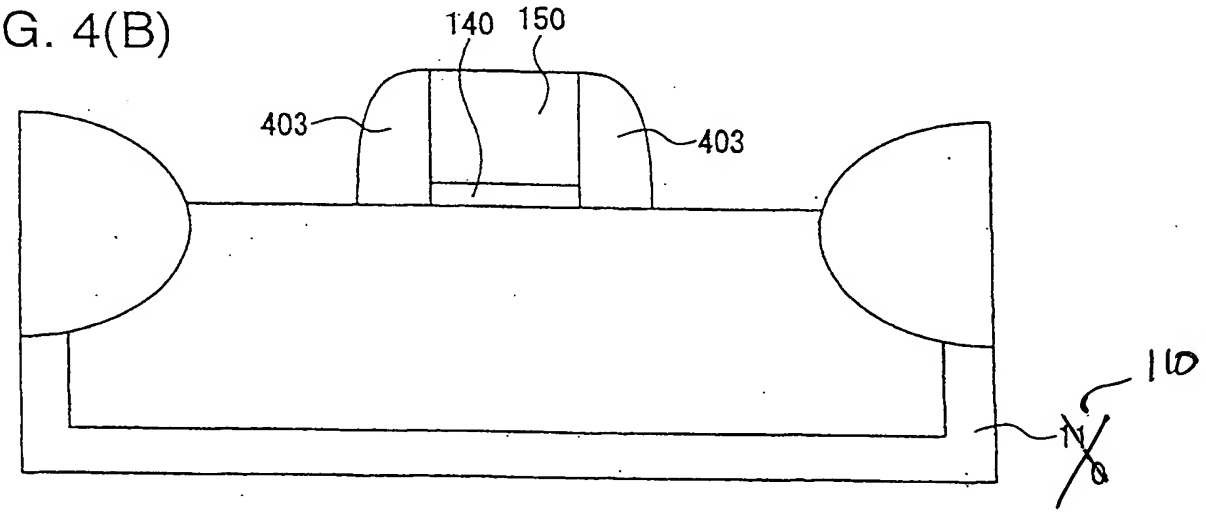
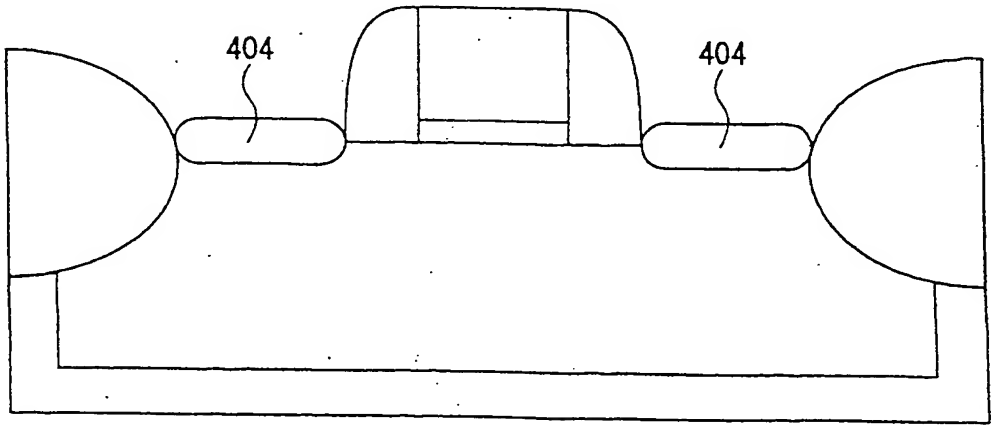


FIG. 4(C)



Process of fabrication of embodiment (a first continuation)